HIGH PERFORMANCE COMPUTING

AMD EPYC™ 7002 SERIES PROCESSORS
REAL WORLD SIMULATION WITH LSTC LS-DYNA®

AMD EPYC

AUGUST 2019

AMD EPYC for HPC

Utilizing the x86 architecture, and built on 7nm technology, the AMD EPYC™ 7002 Series processors bring together high core counts, large memory capacity, extreme memory bandwidth and massive I/O with the right ratios to enable exceptional HPC workload performance.

Standards-Based Architecture

Continuing the AMD commitment to industry standards, AMD EPYC™ 7002 Series processors offer you a choice in x86 architecture. x86 compatibility means you can run most x86-based applications on AMD EPYC processors.

Exceptional Scalability

Scaling is critical to HPC applications. AMD EPYC 7002 Series processors provide high bandwidth between nodes with support for PCIe Gen 4 enabled network devices. Within a node, take advantage of up to 64 cores per socket, including 8 memory channels utilizing speeds up to DDR4-3200[2]. Add incredible floating point and integer compute within each core and the AMD EPYC 7002 Series delivers exceptional performance and scalability for HPC.

LSTC LS-DYNA® and AMD

AMD and LSTC have collaborated to optimize LS-DYNA® on AMD EPYC based systems. The jointly engineered result is high performing and scalable to a large number of processor cores which helps automotive companies and their suppliers test car designs without having to tool or experimentally test a physical prototype, thus saving time and expense.

AMD EPYC™ 7002 Processors: Architectural Innovations Deliver Exceptional Performance and Scalability

The high-performance computing (HPC) market has grown to a point where it is a critical component of new technology advancements in academia and a wide array of industries in both the public and private sectors. Scientific research, public health, climate modeling, and oil and gas exploration are just a few examples where HPC is the driving force behind new innovations and knowledge discovery.

7 nm	PCIe® Gen 4	DDR4 3200
64 Cores per socket	**128** PCIe® Gen 4 lanes per socket	**8** Memory channels per socket
World's first 7 nm x86 server CPU Highest available core count[1] to maximize parallelism	World's first PCIe® Gen 4 ready x86 server CPU[2] Doubles the bandwidth of the previous generation	World's first x86 architecture with DRR4 3200[2] Up to 4 TB of memory capacity per socket

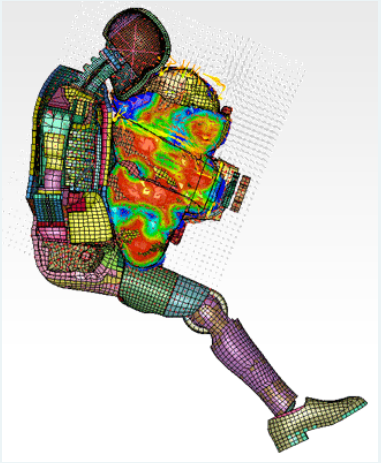
The second generation of the AMD EPYC™ processor extends AMD innovation leadership for HPC. Built with leading-edge 7nm technology, the AMD EPYC™ SoC offers a consistent set of features across a range of choices from 8 to 64 cores, including 128 lanes of PCIe® Gen 4[2] and 8 memory channels with access to up to 4 TB of high-speed memory.

The AMD EPYC™ 7002 Series processor's innovative architecture translates to tremendous performance and scalability for HPC applications, offering you a choice in x86 architecture while optimizing total cost of ownership.

LSTC LS-DYNA®

LS-DYNA® is a general-purpose multi-physics, finite element analysis program capable of simulating complex real-world problems. It is used by the automotive, aerospace, construction, military, manufacturing, and bioengineering industries.

LS-DYNA® is widely used by the automotive industry to analyze vehicle designs. LS-DYNA® accurately predicts a car's behavior in a collision and the effects of the collision upon the car's occupants.



With LS-DYNA, automotive companies and their suppliers can test car designs without having to tool or experimentally test a prototype, thus saving time and expense.

AMD and LSTC have continued their partnership, now certifying LS-DYNA® on AMD EPYC processor-based systems beginning with LS-DYNA® version R9.3.0.

Power without Compromise

Memory bandwidth is a critical factor in maximizing the performance of explicit Finite Element Analysis (FEA) workloads. AMD EPYC server processors' exceptional memory bandwidth helps ensure that you get the most out of your system, optimizing execution time and overall utilization of your deployment.

Many high-performance computing (HPC) workloads require you to balance performance vs. per-core license costs to manage your overall cost. AMD EPYC processors offer a consistent set of features across the product line, allowing users to optimize the number of cores required for their workloads without sacrificing features, memory channels, memory capacity, or I/O lanes. Regardless of the number of physical cores per socket, you will have access to 8 channels of memory per processor across all EPYC server processors.

As workloads demand more processor cores, communication between processor cores becomes critical to efficiently solving the complex problems faced by customers. As cluster sizes increase, communication requirements between nodes rises quickly and can limit scaling at large node counts. AMD and LSTC have collaborated to offer solutions for FEA workloads enabling exceptional performance and low implementation costs.

Performance Testing

This document focuses on performance and scaling of the EPYC 7002 Series Processors. Testing was performed on a cluster of dual-socket EPYC™ 7742-based systems and dual-socket EPYC™ 7542-based systems.

Each EPYC 7742 processor has 64 cores with a base frequency of 2.25 GHz and a boost frequency of 3.4 GHz. Each EPYC 7542 processor has 32 cores with a base frequency of 2.9 GHz and boost of 3.4 GHz.

The compute nodes in the cluster are each populated with 1 DIMM per channel of 64-GB, dual-rank, DDR4-3200 DIMMs from Micron®, for a total of 1TB of memory per node.

A Mellanox® ConnectX-6 200 Gb/s HDR InfiniBand adapter, utilizing EPYC processors' support for PCIe Gen 4, is also populated on each EPYC processor-based system.

Single-node testing was also performed on a 2-socket platform using 1st Gen EPYC 7601 processors to show generational comparisons. Multi-node scaling was then tested on the EPYC 7742 processor.

LS-DYNA® uses a standard set of automotive crash simulation models to measure performance. These models are specifically created to reflect real-world workloads to give a standard basis of comparison across various computer systems and architectures.

The single-node performance tests in this document are using the neon, 3-cars, and car2car models. Scalability results shown for the EPYC 7742 are using the much larger ODB-10M model. All models were downloaded from TopCrunch.org*. The ODB-10M model has 10M cells and is the largest and most representative of today's real-

world car crash simulation models from TopCrunch.org. These models provide a standard baseline for comparing cluster-level performance and scalability of LS-DYNA®. Find the details of the models here.

Tested Hardware and Software Configuration

All testing was done using LS-DYNA version R9.3.0 in a pure MPI configuration using platform MPI. The binary was compiled with avx2 enabled and uses single precision. Planned future testing will include hybrid MPI/OpenMP configurations.

2nd Gen AMD EPYC Compute Nodes		
CPUs	2 x EPYC 7742	2 x EPYC 7542
Cores	64 cores per socket (128 per node)	32 cores per socket (64 per node)
Memory	Micron 1 TB (16x) Dual-Rank DDR4-3200, 1DPC	
Network Adapter	Mellanox ConnectX-6 200Gb/s HDR InfiniBand x16 PCIe® Gen 4	
Storage: OS | Data	1 x Micron 1100 256 GB SATA | 1 x 1 TB NVMe	
Software		
OS	RHEL 7.6 (3.10.0-862.el7.x86_64)	
Mellanox OFED Driver	MLNX_OFED_LINUX-4.5-1.0.1.0 (OFED-4.5-1.0.1)	
Network		
Switch	Mellanox HDR 200Gb/s Unmanaged Switch (MQM8790)	
Configuration Options		
BIOS Setting	NPS = NPS4, SMT = Off, Boost = On, X2APIC = On, Determinism Slider = Performance, Preferred IO=Enabled	
OS Settings	Governor=Performance, CC6 = Disabled	

1st Gen AMD EPYC Compute Nodes	
CPUs	2 x EPYC 7601
Cores	32 cores per socket (64 per node)
Memory	256GB (16x 16GB Dual-Rank) DDR4-2666
NIC	Mellanox ConnectX-5 EDR 100Gb InfiniBand x16 PCIe
Storage: OS | Data	1 x 256 GB NVMe | 1 x 1 TB NVMe
Software	
OS	RHEL 7.6 (3.10.0-862.el7.x86_64)
Mellanox OFED Driver	MLNX_OFED_LINUX-4.5-1.0.1.0 (OFED-4.5-1.0.1)
Network	
Switch	Mellanox HDR 200Gb/s Unmanaged Switch (MQM8790)
Configuration Options	
BIOS Setting	SMT = Off, Boost = On, Determinism Slider = Performance, Global C-State Control = Enabled
OS Settings	Governor=Performance, CC6 = Disabled

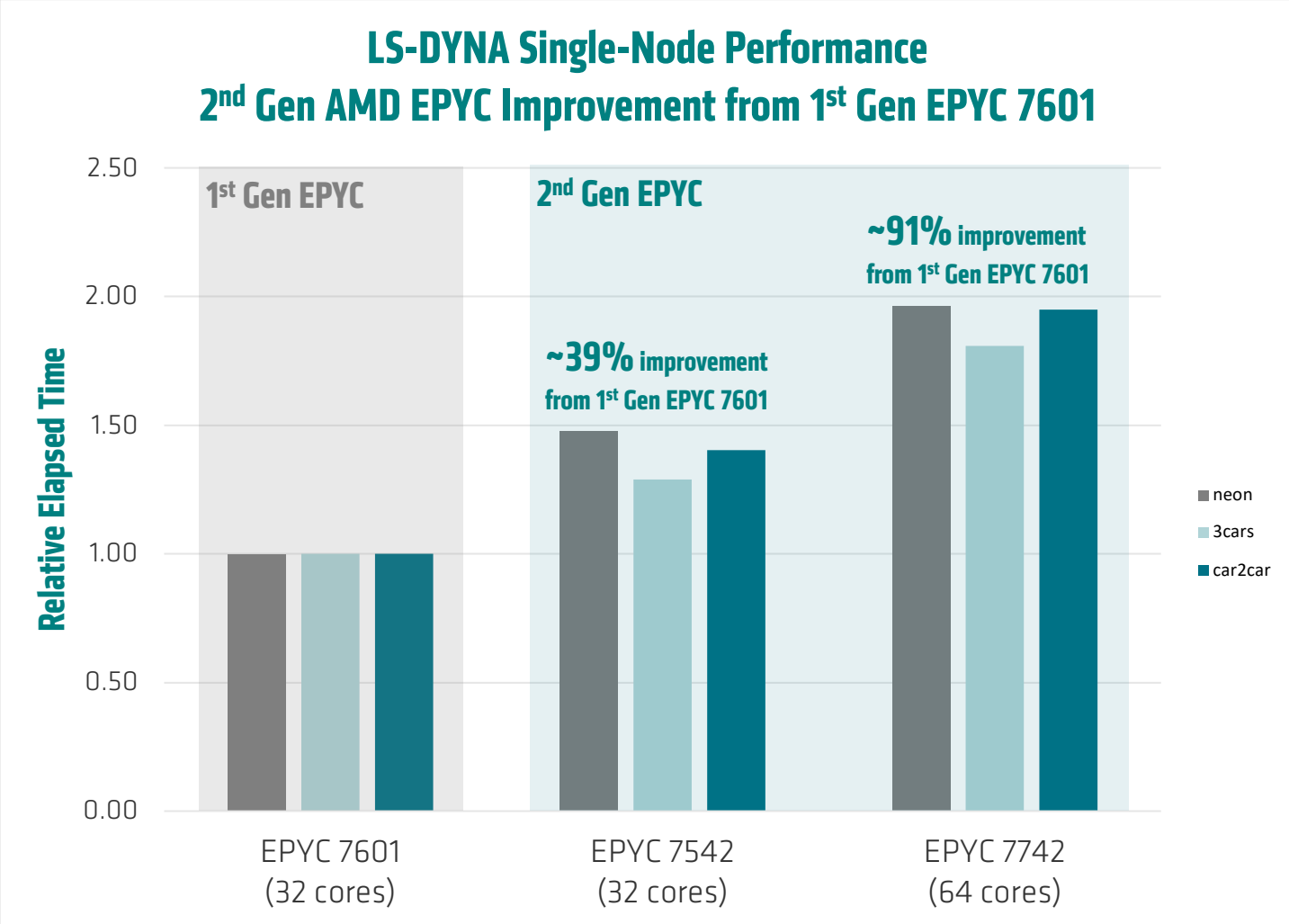
LSTC LS-DYNA: Single-node Performance

The first tests conducted were single node runs across all the benchmarks on the following processors:

- 2nd Generation AMD EPYC 7742 processors (64-core, 2.25 GHz/3.4 GHz)
- 2nd Generation AMD EPYC 7542 processors (32-core, 2.9 GHz/3.4 GHz)
- 1st Generation AMD EPYC 7601 processors (32-core, 2.2 GHz/3.2 GHz)

The results show the AMD EPYC 7742, with 64 cores per socket, has the highest performance. It has an average performance advantage of ~91% higher than the 1st Generation EPYC 7601, with a peak of ~96% higher. Next is the 32-core AMD EPYC 7542. It maintains an average performance advantage of ~39% over the 1st Generation EPYC 7601, with a peak of ~48% higher.

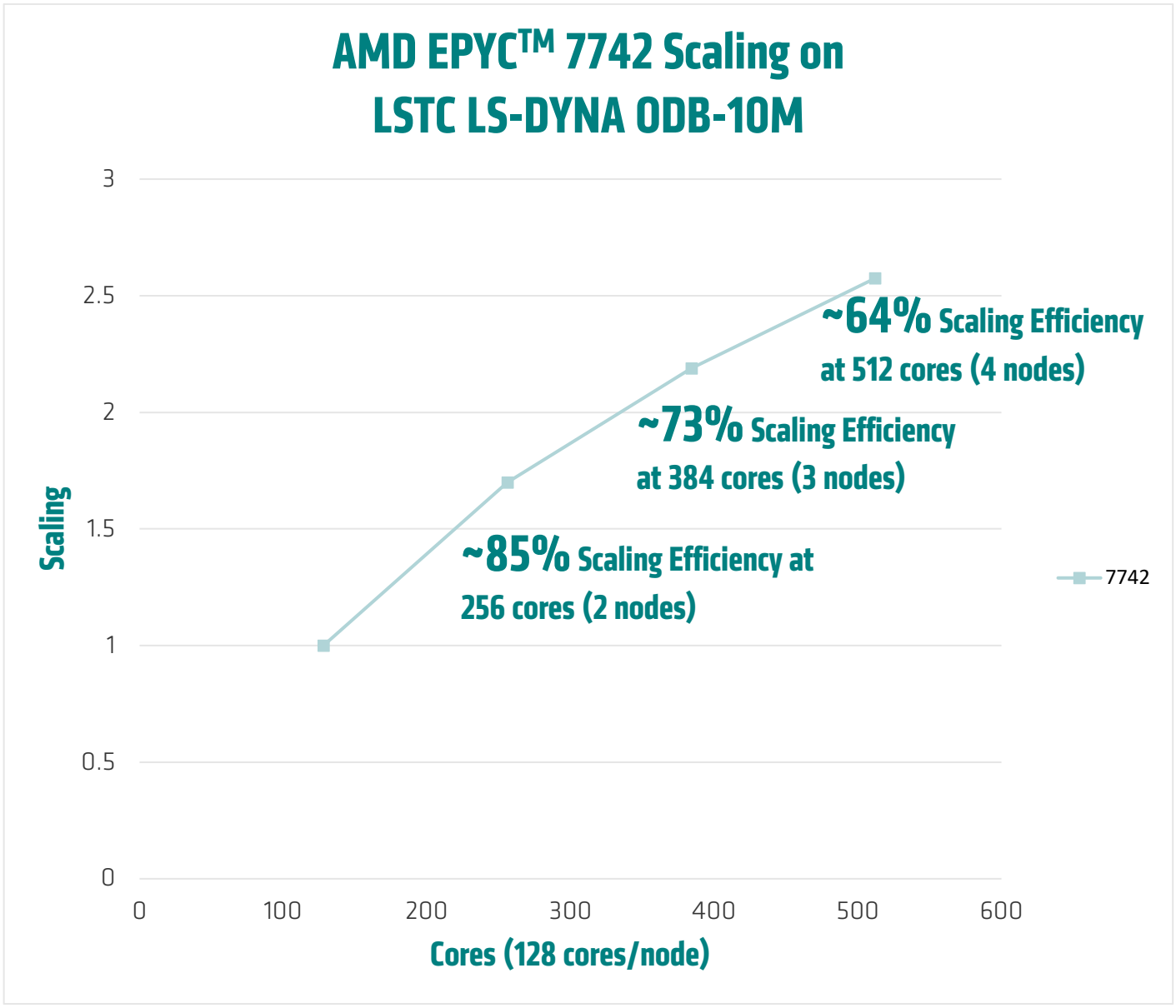
EPYC 7002 Series Processors deliver impressive per-node performance.



LSTC LS-DYNA: Multi-node Scaling

Finite element analysis workloads are complex and require finding the right balance of floating-point performance, memory bandwidth, and network bandwidth. Many FEA clusters use lower core-count processors to balance the memory, IO, and floating-point performance of each node against the communication demands between the nodes. Eight lanes of memory bandwidth on 1st Gen AMD EPYC server processors tilted the balance of system performance. Now, with the 2nd Gen AMD EPYC processors, even more cores, higher compute per core[3], and the addition of PCIe Gen 4 are changing the game again.

128 core jobs hit a sweet spot for FEA explicit workloads today. Putting all 128 cores into a single node creates an ideal configuration. 128 cores/node also allows much better scaling between nodes when combined with a high-performance interconnect (fewer nodes equal less communication overhead). PCIe Gen 4 combined with Mellanox HDR 200Gbps interconnect adds great scalability on an already great compute node. Starting with the highest per-node performance, then scaling at ~85% for 256 cores, or ~73% at 384 cores, provides the ability run larger models at finer granularity in less time. All this in a pure MPI configuration. Planned future testing will include hybrid MPI/OpenMP configurations to further improve scaling.



Conclusion

FEA workloads are demanding and require a balance of memory bandwidth, floating-point performance, and network IO. 2nd Gen AMD EPYC processors provide exceptional memory bandwidth, high floating-point performance, and incredibly fast I/O with Mellanox 200Gb/s HDR InfiniBand networking, delivering a dominating combination of features and raw compute power to tackle today's, and tomorrow's, FEA workloads.

As demanding FEA workloads scale-out to more threads, inter-process communication requirements can increase dramatically. Moving more of those threads into each system shifts more of the inter-process communication to happen within each node, driving higher per-system performance and density. Whether you are scaling-out to higher node-counts, or driving more density into your clusters, AMD EPYC 7002 Series processors give you more levers to tilt the performance balance your way. This provides new opportunities for more density in your datacenter, and for even more demanding FEA workloads.

LSTC LS-DYNA® Finite Element Analysis application is architected to deliver accuracy, performance, and scalability. The automotive industry relies upon LS-DYNA® to accurately simulate cars' behavior in collisions, allowing increased safety, reduced development costs, and quicker time to production.

Together, AMD and LSTC empower the development of faster, more accurate finite element analysis simulations running on cost-effective clustered systems.

For more information about AMD's EPYC line of processors visit: http://www.amd.com/epyc

For more information about LSTC visit: http://www.lstc.com

* Links to third party sites are provided for convenience and unless explicitly stated, AMD is not responsible for the contents of such linked sites and no endorsement is implied. GD-5

FOOTNOTES

1. Best-in-class based on industry-standard pin-based (LGA) X86 processors. NAP-166.
2. Some supported features and functionality of second-generation AMD EPYC™ processors (codenamed "Rome") require a BIOS update from your server manufacturer when used with a motherboard designed for the first-generation AMD EPYC 7000 series processor. A motherboard designed for "Rome" processors is required to enable all available functionality. ROM-06.
3. A "Zen2" based processor has a theoretical peak of ~4X Floating Point Per Socket (FLOPS) more than a "Zen1" based processor. Determined by typical industry calculation method for FLOPS, ROM-04